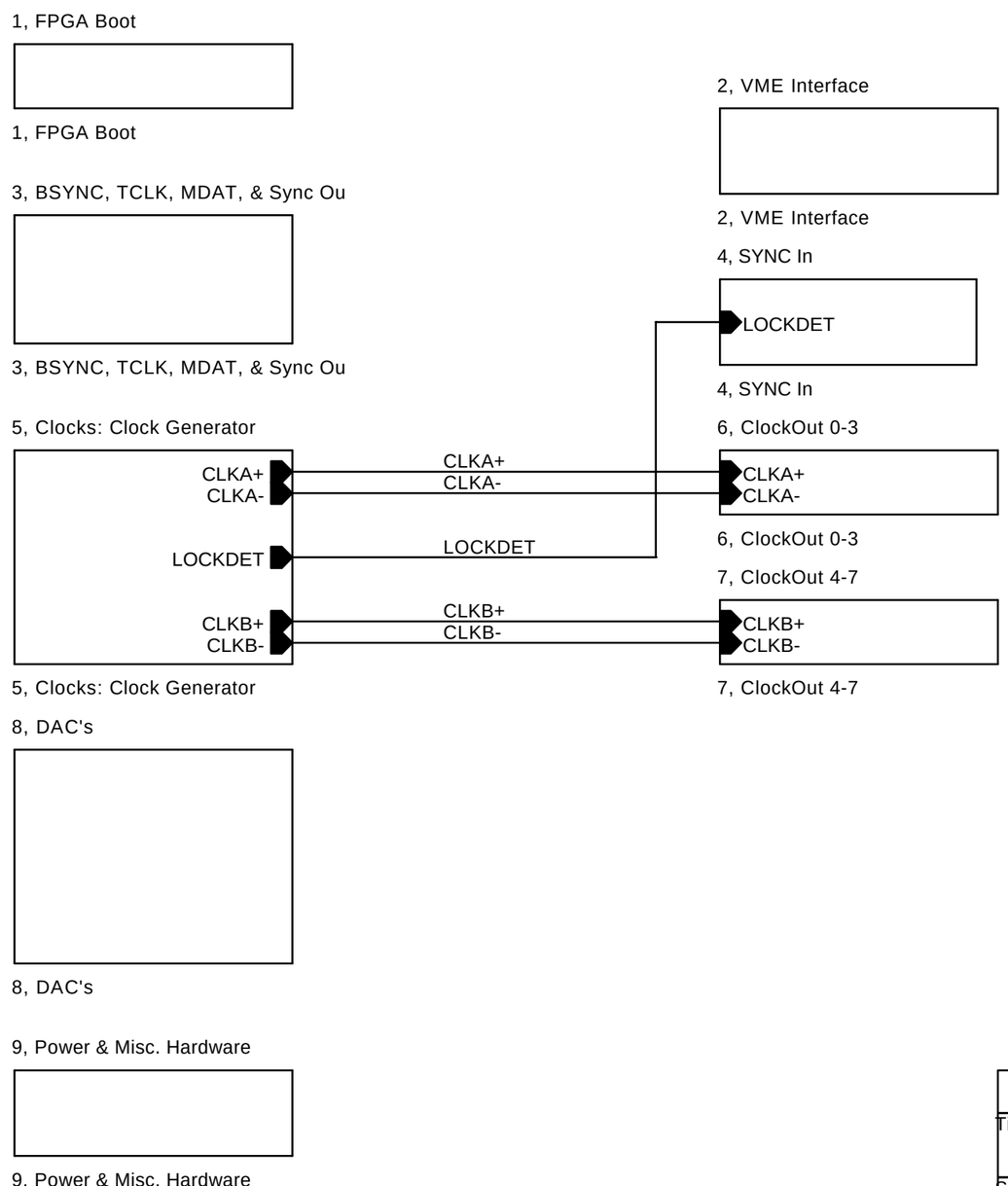
Timing Generator Fanout Card



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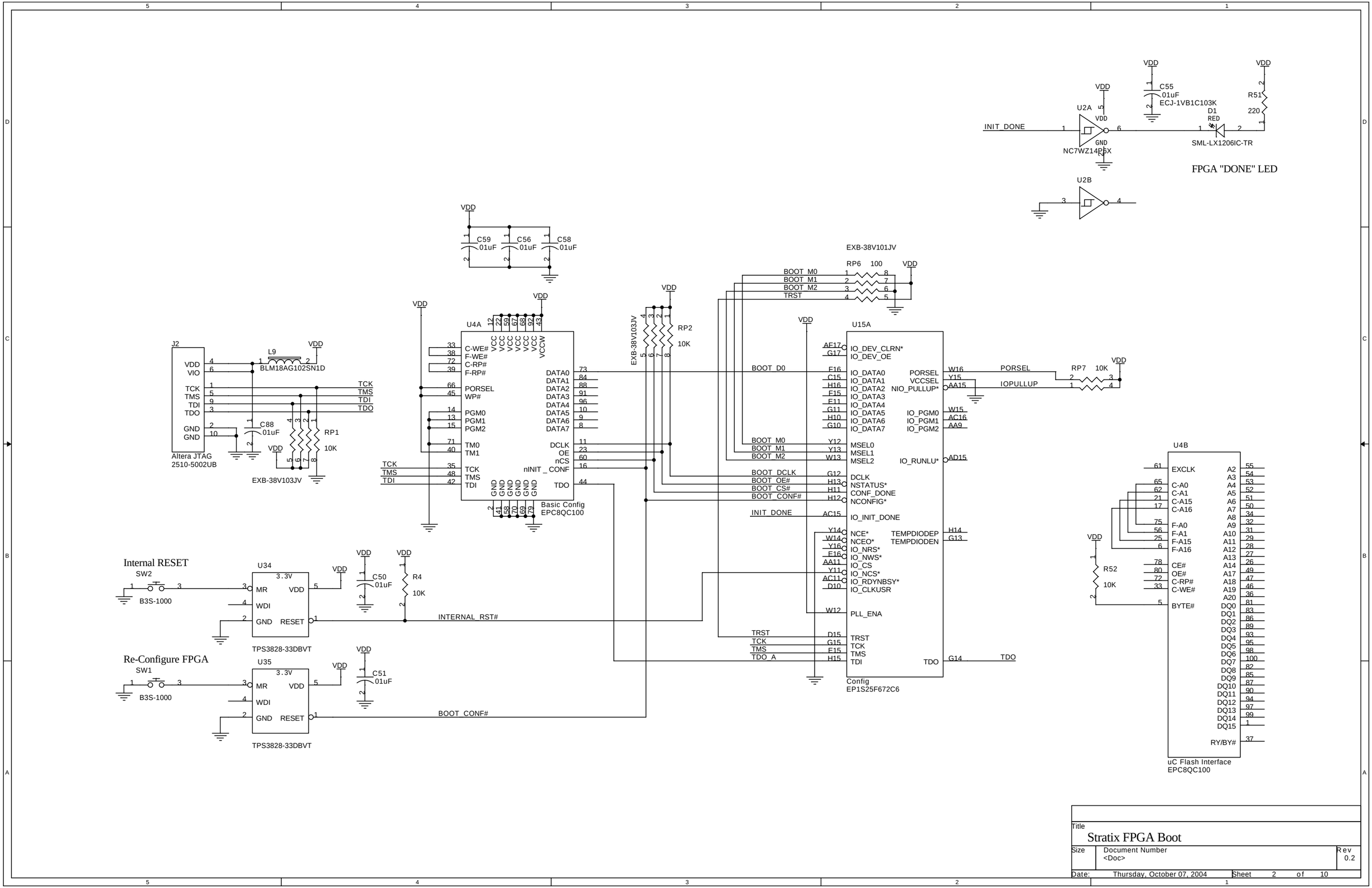
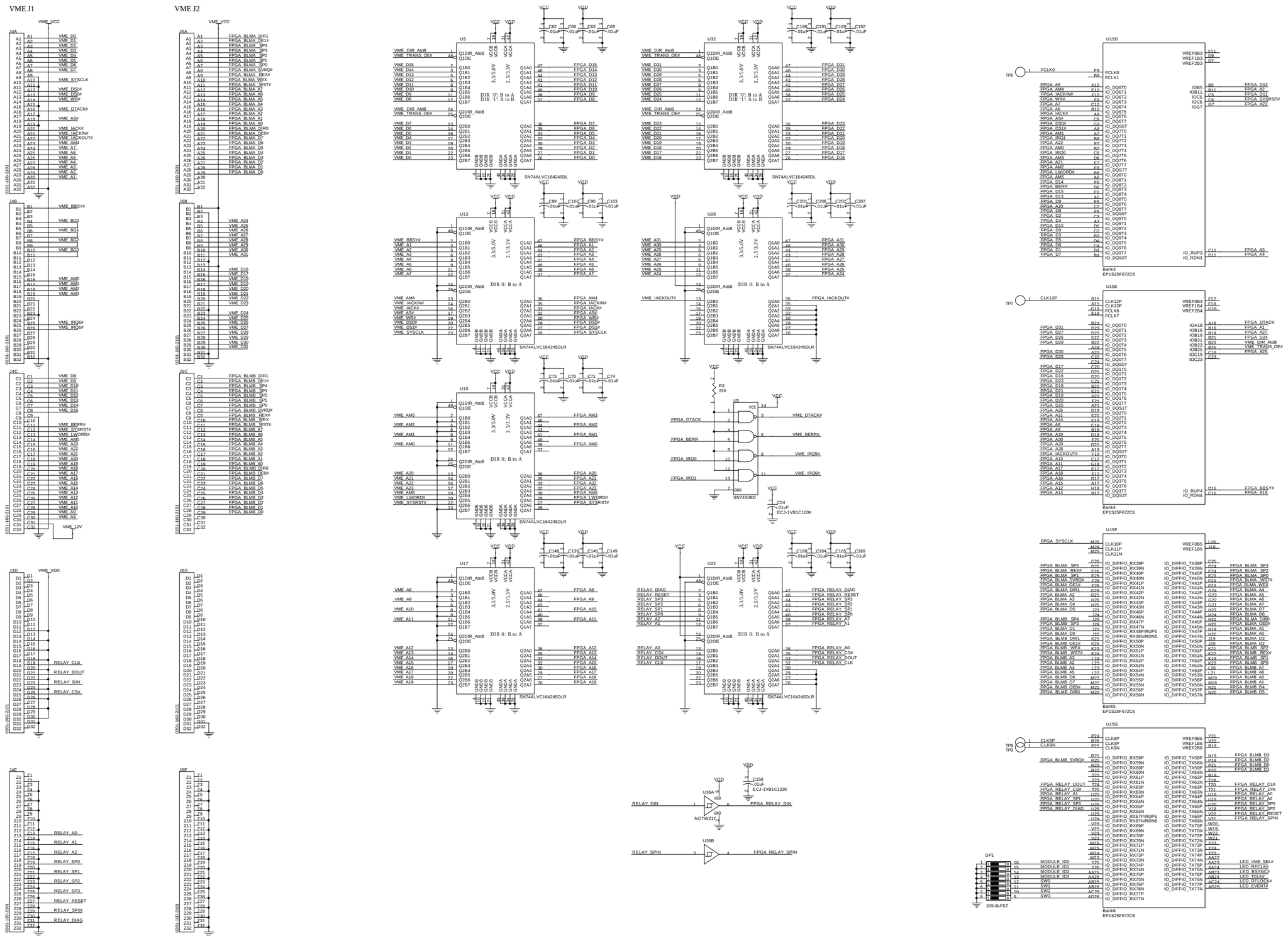
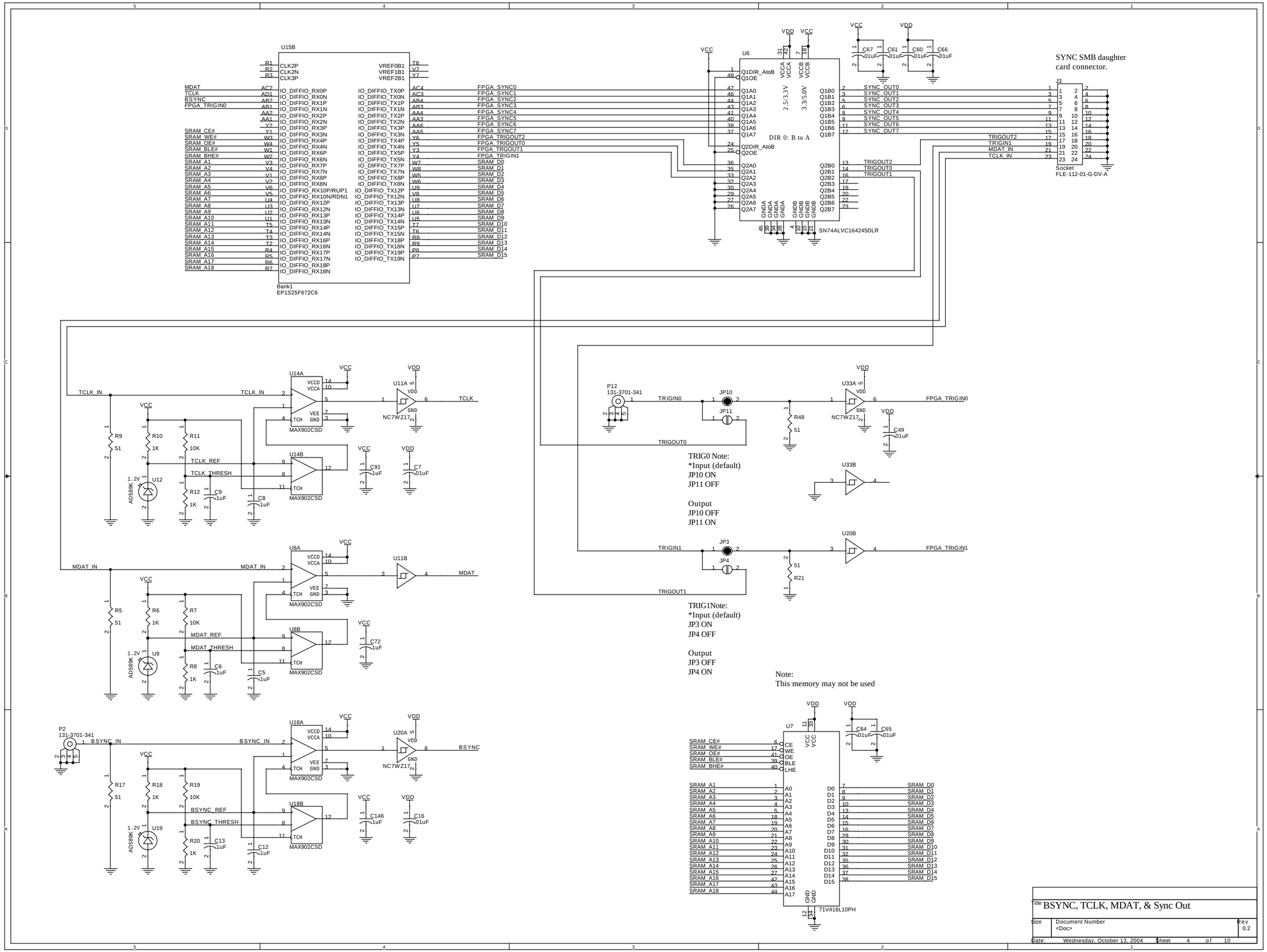
Size: A	Document Number: <Doc>	Rev: 0.2
Date: Monday, October 04, 2004	Sheet 1 of 10	


FPGA "DONE" LED
INIT_DONE
U2A
NC7WZ14P5X
U2B
C55
01uF
ECJ-1VB1C103K
D1
RED
SML-LX1206IC-TR
R51
220
VDD
C59
01uF
C56
01uF
C58
01uF
J2
Altera JTAG
2510-5002UB
L9
BLM18AG102SN1D
C88
01uF
RP1
10K
EXB-38V103JV
U4A
Basic Config
EPC8QC100
RP2
10K
EXB-38V101JV
RP6 100
BOOT_M0
BOOT_M1
BOOT_M2
TRST
U15A
Config
EP1S25F672C6
RP7 10K
PORSEL
IOPULLUP
TDO
U4B
uC Flash Interface
EPC8QC100
R52
10K
Internal RESET
SW2
B3S-1000
U34
TPS3828-33DBVT
C50
01uF
R4
10K
INTERNAL_RST#
Re-Configure FPGA
SW1
B3S-1000
U35
TPS3828-33DBVT
C51
01uF
BOOT_CONF#
Title
Stratix FPGA Boot
Size
Document Number
<Doc>
Rev
0.2
Date: Thursday, October 07, 2004
Sheet 2 of 10


VME J1
VME J2
U5
U13
U10
U17
U32
U28
U22
U15D
U15E
U15F
U15G
U36A
U36B
U3
DP1
Status LED's
Bank3
EP1S25F672C6
Bank4
EP1S25F672C6
Bank5
EP1S25F672C6
Bank6
EP1S25F672C6
SN74ALVC164245DL
SN74ALVC164245DLR
SN74S38D
NC7WZ17
209-8LPST
Title
VME Interface
Size D
Document Number <Doc>
Rev 0.2
Date: Friday, October 08, 2004
Sheet 3 of 10


U15B
Bank1
EP1S25F672C6
U6
SN74ALVC164245DLR
DIR 0: B to A
2.5/3.3V
3.3/5.0V
SYNC SMB daughter card connector.
J3
Socket
FLE-112-01-G-DV-A
MDAT
TCLK
BSYNC
FPGA_TRIGIN0
SRAM_CE#
SRAM_WE#
SRAM_OE#
SRAM_BLE#
SRAM_BHE#
FPGA_SYNC0
FPGA_SYNC1
FPGA_SYNC2
FPGA_SYNC3
FPGA_SYNC4
FPGA_SYNC5
FPGA_SYNC6
FPGA_SYNC7
FPGA_TRIGOUT2
FPGA_TRIGOUT0
FPGA_TRGOUT1
FPGA_TRIGIN1
SYNC_OUT0
SYNC_OUT1
SYNC_OUT2
SYNC_OUT3
SYNC_OUT4
SYNC_OUT5
SYNC_OUT6
SYNC_OUT7
TRIGOUT2
TRIGIN1
MDAT_IN
TCLK_IN
TRIGOUT0
TRIGOUT1
U14A
U14B
MAX902CSD
U11A
NC7WZ17
TCLK
TCLK_REF
TCLK_THRESH
U12
AD589K
P12
131-3701-341
JP10
JP11
U33A
U33B
FPGA_TRIGIN0
TRIG0 Note:
*Input (default)
JP10 ON
JP11 OFF
Output
JP10 OFF
JP11 ON
JP3
JP4
U20B
FPGA_TRIGIN1
TRIG1Note:
*Input (default)
JP3 ON
JP4 OFF
Output
JP3 OFF
JP4 ON
U8A
U8B
U11B
MDAT
MDAT_REF
MDAT_THRESH
U9
P2
131-3701-341
BSYNC_IN
U18A
U18B
U20A
BSYNC
BSYNC_REF
BSYNC_THRESH
U19
Note:
This memory may not be used
U7
71V416L10PH
Title
BSYNC, TCLK, MDAT, & Sync Out
Size
Document Number
<Doc>
Rev
0.2
Date:
Wednesday, October 13, 2004
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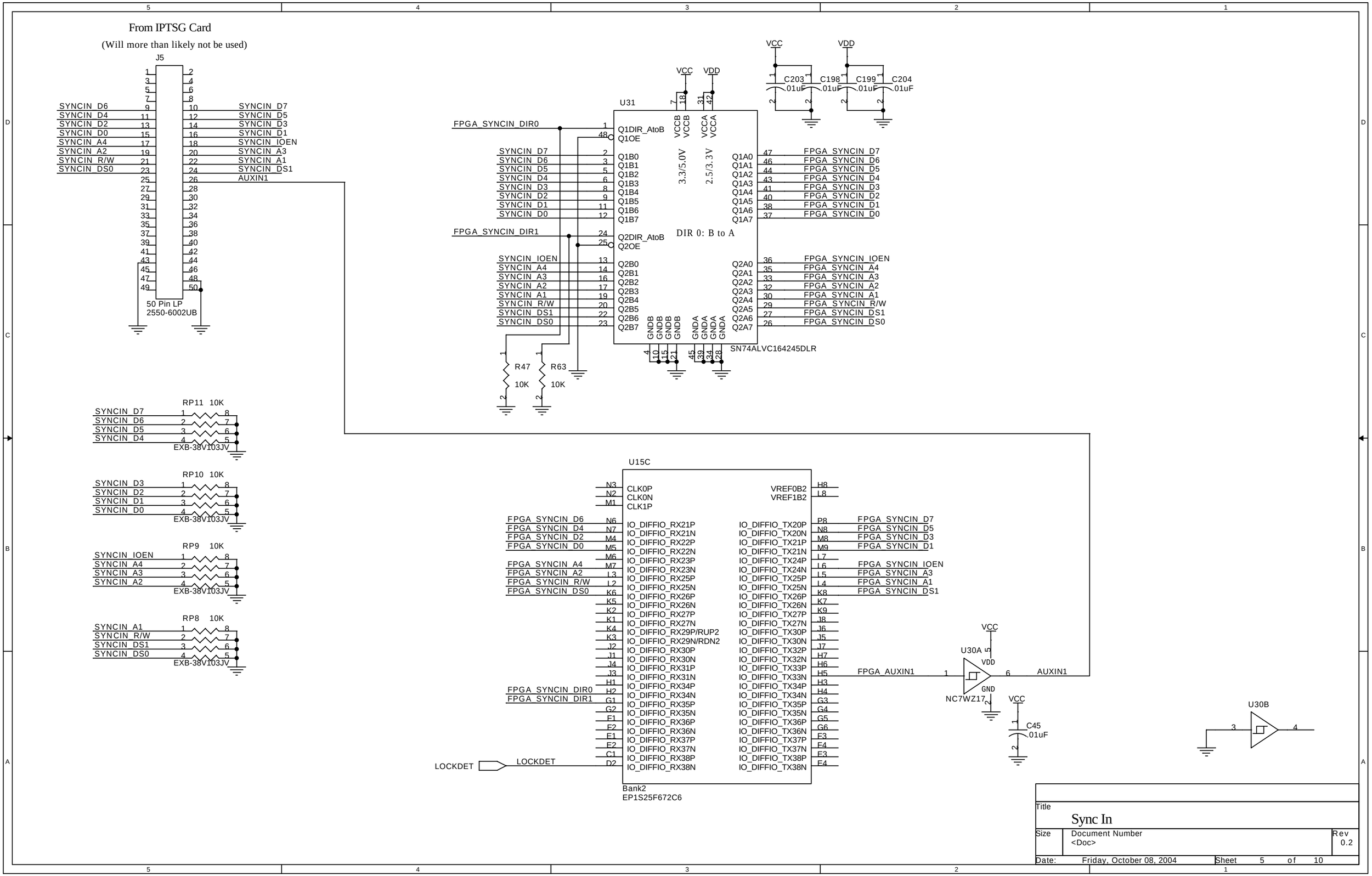
4
of
10


From IPTSG Card
(Will more than likely not be used)
J5
50 Pin LP
2550-6002UB
SYNCIN_D6
SYNCIN_D4
SYNCIN_D2
SYNCIN_D0
SYNCIN_A4
SYNCIN_A2
SYNCIN_R/W
SYNCIN_DS0
SYNCIN_D7
SYNCIN_D5
SYNCIN_D3
SYNCIN_D1
SYNCIN_IOEN
SYNCIN_A3
SYNCIN_A1
SYNCIN_DS1
AUXIN1
U31
SN74ALVC164245DLR
DIR 0: B to A
3.3/5.0V
2.5/3.3V
FPGA_SYNCIN_DIR0
FPGA_SYNCIN_DIR1
FPGA_SYNCIN_D7
FPGA_SYNCIN_D6
FPGA_SYNCIN_D5
FPGA_SYNCIN_D4
FPGA_SYNCIN_D3
FPGA_SYNCIN_D2
FPGA_SYNCIN_D1
FPGA_SYNCIN_D0
FPGA_SYNCIN_IOEN
FPGA_SYNCIN_A4
FPGA_SYNCIN_A3
FPGA_SYNCIN_A2
FPGA_SYNCIN_A1
FPGA_SYNCIN_R/W
FPGA_SYNCIN_DS1
FPGA_SYNCIN_DS0
VCC
VDD
C203 .01uF
C198 .01uF
C199 .01uF
C204 .01uF
R47 10K
R63 10K
RP11 10K
RP10 10K
RP9 10K
RP8 10K
EXB-38V103JV
U15C
Bank2
EP1S25F672C6
CLK0P
CLK0N
CLK1P
VREF0B2
VREF1B2
LOCKDET
FPGA_AUXIN1
AUXIN1
U30A
NC7WZ17
C45 .01uF
U30B
Title
Sync In
Size
Document Number
<Doc>
Rev
0.2
Date: Friday, October 08, 2004
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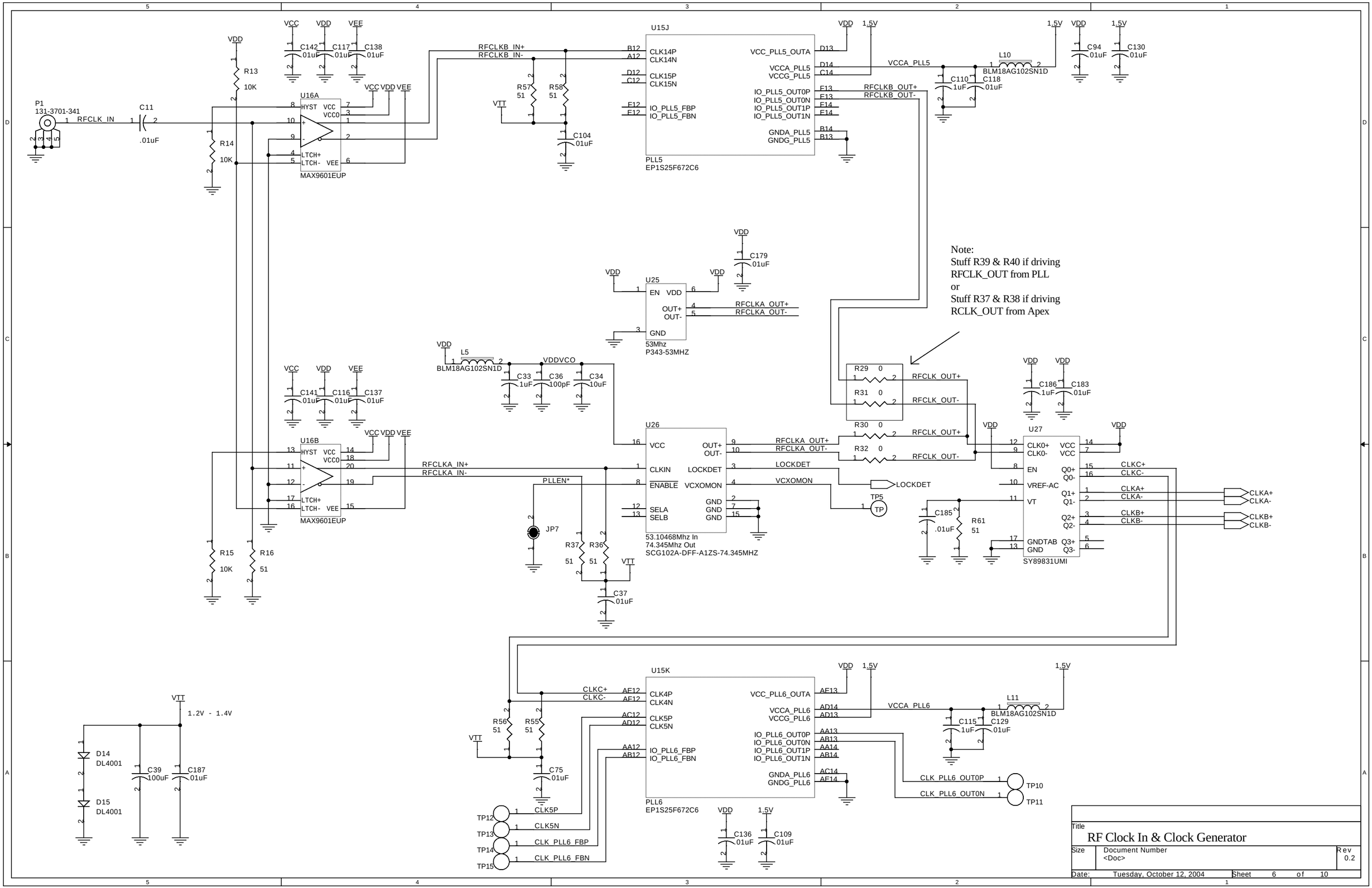
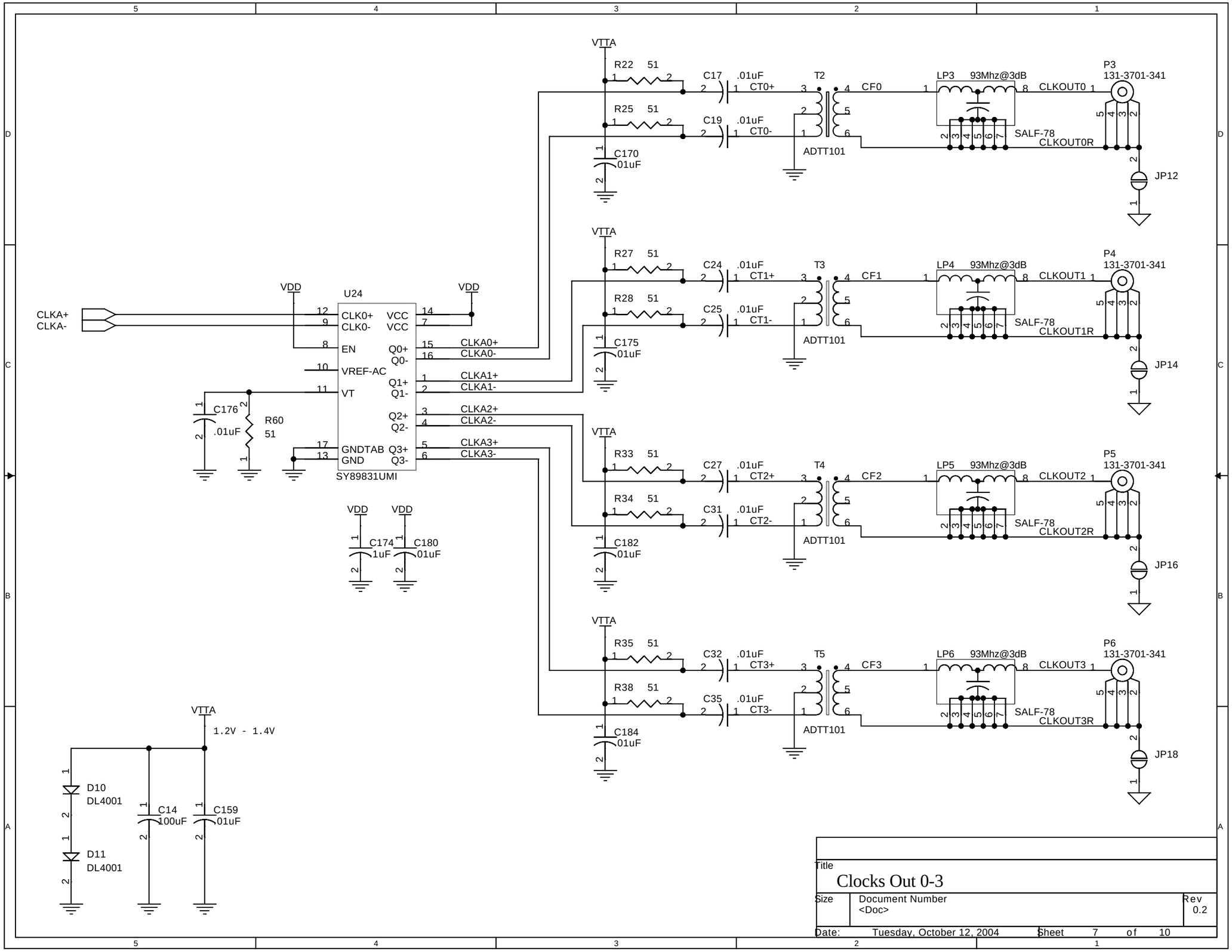


Title
RF Clock In & Clock Generator

Size	Document Number	Rev
	<Doc>	0.2

Date: Tuesday, October 12, 2004 Sheet 6 of 10


VTTA
R22 51
C17 .01uF
CT0+
T2
CF0
LP3 93Mhz@3dB
CLKOUT0
P3
131-3701-341
R25 51
C19 .01uF
CT0-
ADTT101
SALF-78
CLKOUT0R
C170
01uF
JP12
R27 51
C24 .01uF
CT1+
T3
CF1
LP4 93Mhz@3dB
CLKOUT1
P4
131-3701-341
R28 51
C25 .01uF
CT1-
ADTT101
SALF-78
CLKOUT1R
C175
01uF
JP14
VDD
U24
CLKA+
CLKA-
CLK0+
CLK0-
EN
VREF-AC
VT
GNDTAB
GND
VCC
Q0+
Q0-
Q1+
Q1-
Q2+
Q2-
Q3+
Q3-
SY89831UMI
CLKA0+
CLKA0-
CLKA1+
CLKA1-
CLKA2+
CLKA2-
CLKA3+
CLKA3-
C176
.01uF
R60
51
C174
1uF
C180
01uF
R33 51
C27 .01uF
CT2+
T4
CF2
LP5 93Mhz@3dB
CLKOUT2
P5
131-3701-341
R34 51
C31 .01uF
CT2-
ADTT101
SALF-78
CLKOUT2R
C182
01uF
JP16
R35 51
C32 .01uF
CT3+
T5
CF3
LP6 93Mhz@3dB
CLKOUT3
P6
131-3701-341
R38 51
C35 .01uF
CT3-
ADTT101
SALF-78
CLKOUT3R
C184
01uF
JP18
1.2V - 1.4V
D10
DL4001
D11
DL4001
C14
100uF
C159
01uF
Title
Clocks Out 0-3
Size
Document Number
<Doc>
Rev
0.2
Date: Tuesday, October 12, 2004
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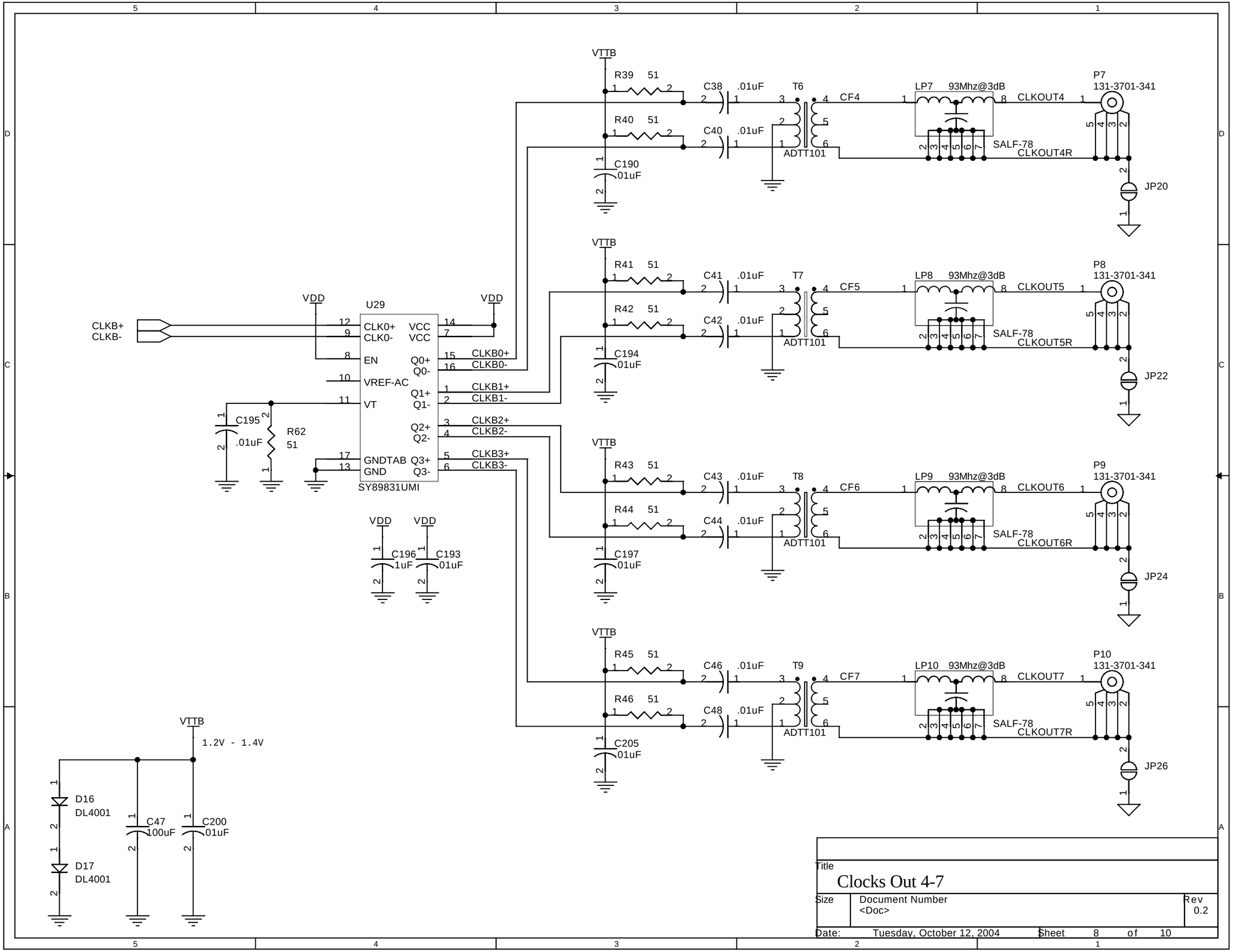

Title
Clocks Out 4-7

Size	Document Number	Rev
	<Doc>	0.2

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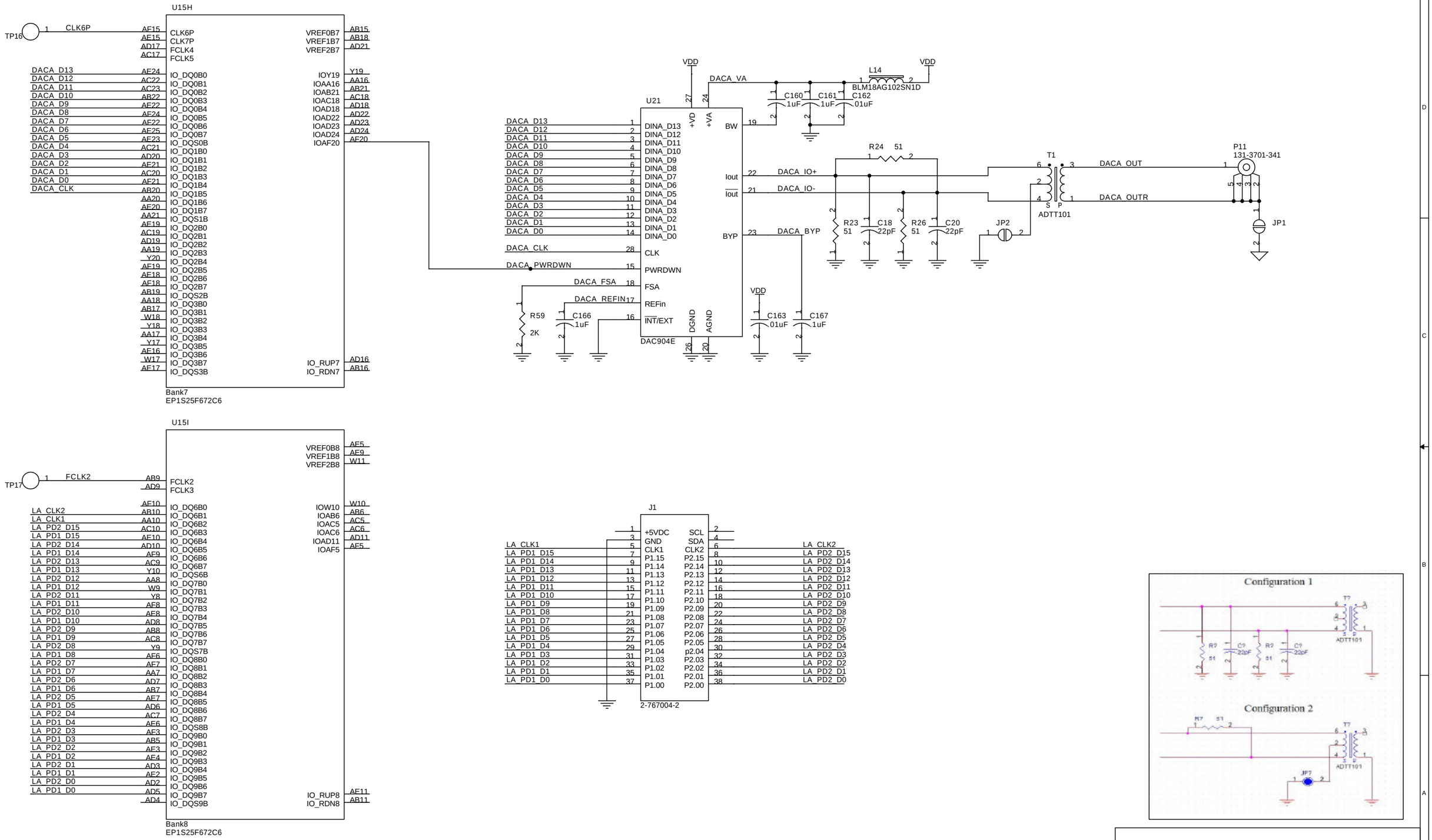

Title
Digital to Analog Outputs

Size	Document Number	Rev
	<Doc>	0.2

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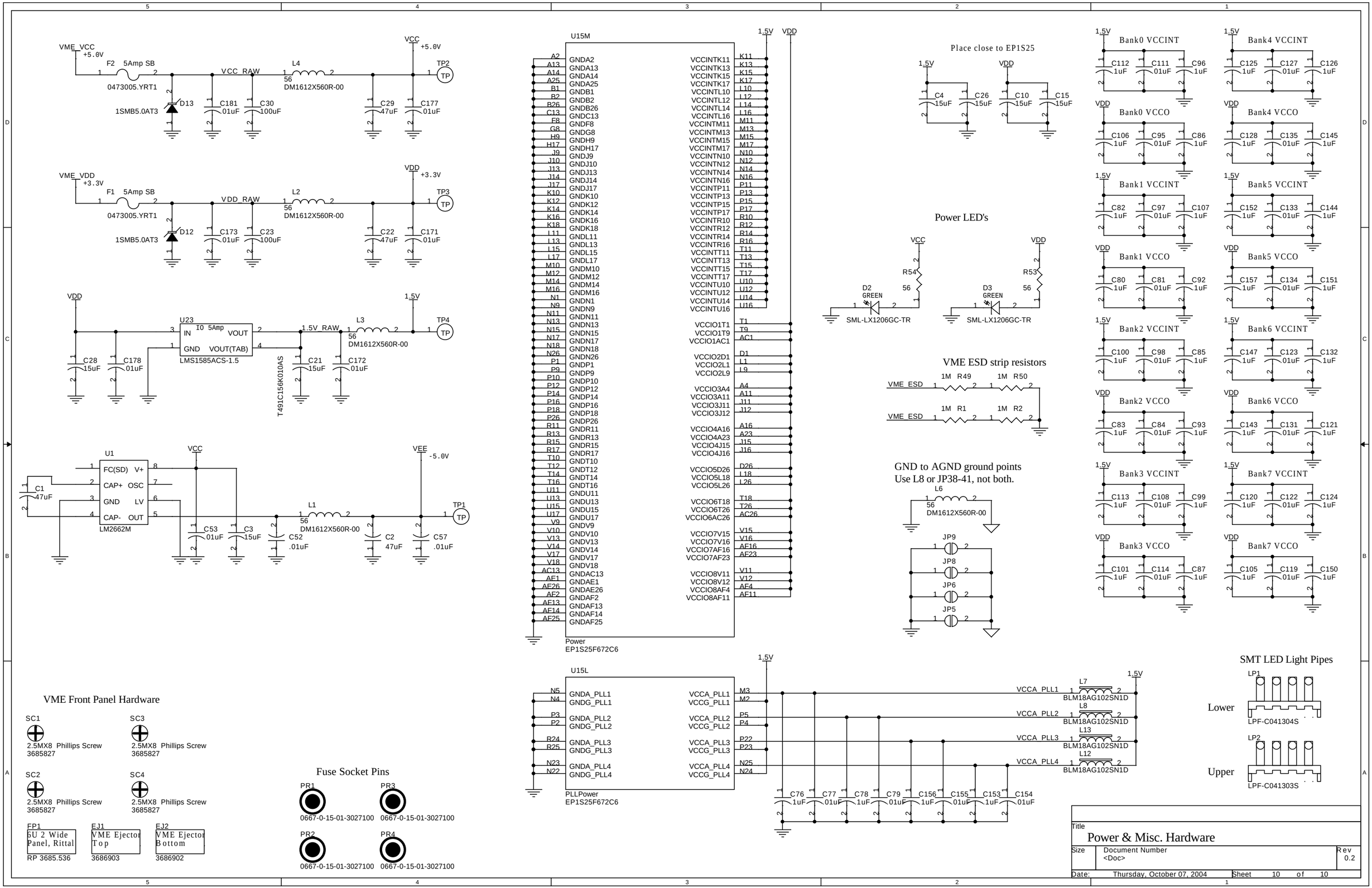
VME_VCC
+5.0V
F2 5Amp SB
0473005.YRT1
VCC_RAW
L4
56
DM1612X560R-00
VCC
+5.0V
TP2
D13
1SMB5.0AT3
C181 01uF
C30 100uF
C29 47uF
C177 01uF
VME_VDD
+3.3V
F1 5Amp SB
0473005.YRT1
VDD_RAW
L2
56
DM1612X560R-00
VDD
+3.3V
TP3
D12
1SMB5.0AT3
C173 01uF
C23 100uF
C22 47uF
C171 01uF
VDD
U23
IO 5Amp
IN
VOUT
GND
VOUT(TAB)
LMS1585ACS-1.5
1.5V_RAW
L3
56
DM1612X560R-00
1.5V
TP4
C28 15uF
C178 01uF
T491C156K010AS
C21 15uF
C172 01uF
U1
FC(SD)
V+
CAP+
OSC
GND
LV
CAP-
OUT
LM2662M
C1 47uF
VCC
VEE
-5.0V
L1
56
DM1612X560R-00
TP1
C53 .01uF
C3 15uF
C52 .01uF
C2 47uF
C57 .01uF
U15M
Power
EP1S25F672C6
1.5V
VDD
Place close to EP1S25
C4 15uF
C26 15uF
C10 15uF
C15 15uF
Power LED's
D2 GREEN
R54 56
SML-LX1206GC-TR
D3 GREEN
R53 56
SML-LX1206GC-TR
VME ESD strip resistors
VME_ESD
1M R49
1M R50
1M R1
1M R2
GND to AGND ground points
Use L8 or JP38-41, not both.
L6
56
DM1612X560R-00
JP9
JP8
JP6
JP5
Bank0 VCCINT
Bank4 VCCINT
Bank0 VCCO
Bank4 VCCO
Bank1 VCCINT
Bank5 VCCINT
Bank1 VCCO
Bank5 VCCO
Bank2 VCCINT
Bank6 VCCINT
Bank2 VCCO
Bank6 VCCO
Bank3 VCCINT
Bank7 VCCINT
Bank3 VCCO
Bank7 VCCO
U15L
PLLPower
EP1S25F672C6
VCCA_PLL1
VCCA_PLL2
VCCA_PLL3
VCCA_PLL4
L7
L8
L13
L12
BLM18AG102SN1D
C76 1uF
C77 01uF
C78 1uF
C79 01uF
C156 1uF
C155 01uF
C153 1uF
C154 01uF
SMT LED Light Pipes
Lower
LP1
LPF-C041304S
Upper
LP2
LPF-C041303S
VME Front Panel Hardware
SC1
SC2
SC3
SC4
2.5MX8 Phillips Screw
3685827
FP1
6U 2 Wide Panel, Rittal
RP 3685.536
EJ1
VME Ejector Top
3686903
EJ2
VME Ejector Bottom
3686902
Fuse Socket Pins
PR1
PR2
PR3
PR4
0667-0-15-01-3027100
Title
Power & Misc. Hardware
Size
Document Number
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Rev
0.2
Date: Thursday, October 07, 2004
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